

## Guest Editorial – Special Issue on ‘Memristors: Devices, Models, Circuits, Systems, and Applications’

As the human society enters the era of ‘big data’, the capacity to generate large amounts of information grows exponentially. Cities across the world are relying upon and consistently generating massive amount of data – traffic navigations, parking managements, energy consumption rates, etc. Overall, the data double in volume every 2 years and are predicted to reach 44 zettabytes by 2020. It should be noted that among the newly created data, only less than 20% of them are well structured and can be readily analyzed by software, while more than 80% of the data are unstructured and cannot be easily recognized and analyzed by existing computers/programs. The high value attached to the high volume and large variety of unstructured data can only be extracted if a proper analysis is possible. In particular, intelligent hardware that spontaneously learns to sort out the structure and information of the data through unsupervised learning is required for the data analytics as the tags regarding the formats and structures of the target data are missing.

Memristor devices embedded in pioneering nanoelectronic platforms represent the most promising key-enabling technology for the treatment of massive amount of data. The memristor, a two-terminal circuit element characterized by a nonlinear relation between the time integrals of current and voltage (i.e., the current and voltage momenta, aka charge and flux), was theoretically envisioned by Prof. L. O. Chua back in 1971. Features of the memristor proposed by Prof. Chua were found in a nanoscale film based on titanium dioxide in 2008 by a team of Hewlett Packard researchers led by S. Williams. This discovery has been recently followed by the experimental observation of some aspects of memristor behavior in other nanostructures. Memristor nanodevices typically adopt a metal/insulator/metal structure. The electrode materials and the switching layer are carefully designed so as to obtain desirable programming voltage, on/off ratio, power consumption, and device variation that enable fast, low-power yet reliable data analysis. Some of these physical devices are capable to reproduce the nonlinear dynamics of neural synapses with high level of accuracy: they may process and store information at the same time, they may occupy nanoscale volumes, they may be arranged on multi-layer crossbar array configurations ideally suited for parallel processing, they may consume very little power, and, most importantly, they may exhibit flux-controllable conductances reminiscent of the ion flow-tunable weights of neural synapses. As an additional benefit, this technology is also enabling non-volatile low-power memories, that are assumed to be one of the possible replacements for current data storage systems.

The COST Action IC1401, ‘Memristors: Devices, Models, Circuits, Systems and Applications (MemoCiS)’, supported by COST (European Cooperation in Science and Technology) is aimed at bringing together researchers of different backgrounds to work in unison, so as to overcome multidisciplinary barriers that exist across the various domains associated with memristors. Most members of the Action work across the workgroups have contributed in this Special Issue and on the progress made with respect to ‘Memristor Device Technology’, ‘Memristor Theory, Modeling, and Simulation’, ‘Memristor-based Circuits’, and ‘Memristive Systems’ (which include bioinspired networks and memristive biosensors).

Since 1974, the International Journal of Circuit Theory and Applications<sup>‡</sup> has been paying attention to bridge gap between the theoretical concept of memristor and its use in Engineering, Physics, and Material Science.

This Special Issue on Memristors: Devices, Models, Circuits, Systems, and Applications is devoted to create a focused forum on the theory of memristor, analysis of complex dynamics in memristor-based circuits and systems, new solutions for memristor fabrication, and their integration in neuromorphic systems, logic gates, and intelligent systems.

<sup>‡</sup>Leon O. Chua and Chong-Wei Tseng, “A memristive circuit model for p-n junction diodes”, Volume 2, Issue 4, December 1974, Pages 367–389.

The paper 'State of the Art and Challenges for Test and Reliability of Emerging Non-volatile Resistive Memories' provides an overview of the main emerging non-volatile memory technologies, phase change memory, resistive random access memory, and spin-transfer-torque random access memory. The work makes available for design and test engineers alike, a comprehensive view of challenges and existing solutions for emerging memories test, design for test, reliability, and design for reliability.

Following the classification of memristor devices introduced in the work 'A theoretical approach to memristor devices', the paper 'Exploring Resistive Switching based Memristors in the Charge-Flux Domain, a Modeling Approach' introduces a model in the charge-flux domain to describe resistive switching memristor operation. The implementation of the flux-charge memristor model into SPICE-like simulators is used then to fit experimental and simulated i-v curves for different reset processes.

The paper 'SPICE simulation of memristive circuits based on memdiodes with sigmoidal threshold functions' presents a SPICE implementation of a memristor model and its use in different memristor-based circuits. The memristor model is based on sigmoidal threshold functions that switch the parameters involved in the transport equation. Results show that the model is stable under different driving signals, in particular, in multi-element circuits. Anti-parallel and anti-series configurations are investigated as well as its application to thresholding devices and memory cells exploiting the memristor/selector structures.

The paper 'Modeling and Simulation of Large Memristive Networks' studies non-convergence and numerical issues in the simulation of networks with an extremely large number of memristors. The behavior in the simulations of three different memristor models when used to solving some benchmark problems is analyzed. Benchmark circuits for testing the applications of various complexities are used for the transient analysis in HSPICE. It is shown how the models can be modified to minimize the simulation time and improve the convergence.

The paper 'Harmonic balance method to analyze bifurcations in memristor oscillatory circuits' studies nonlinear dynamics and bifurcations of a class of memristor oscillatory circuits obtained by replacing the nonlinear resistor of a Chua's oscillator with a flux-controlled memristor. A recently developed technique, named Flux-Charge Analysis Method, has shown that the state space of such circuits can be decomposed in invariant manifolds, where each manifold is characterized by a different dynamics and different attractors. The use of the Harmonic Balance method in combination with Flux-Charge Analysis Method in order to study the different kinds of bifurcations generated by changing the circuit parameters on a fixed manifold, changing manifold for a fixed parameter set (bifurcations without parameters), or changing simultaneously circuit parameters and manifolds.

The paper 'A novel no-equilibrium hyperchaotic multi-wing system via introducing memristor' introduces a new multi-wing chaotic attractor and a novel method to generate hyperchaotic multi-wing attractors. Interestingly, the proposed memristor-based system exhibits a hyperchaotic multi-wing attractor, but it has no-equilibrium. The phase portraits and Lyapunov exponents are used to analyze the dynamic behaviors of the no-equilibrium memristive system. The electronic circuit can be realized by using off-the-shelf components.

The paper 'Case Study on Memristor-Based Multilevel Memories' the authors have designed a few concise and high performance circuits to support and expand the usage of memristor, especially for multi-level memristors. In the circuit integration part, the ADC is realized by using a different width ratio of inverters with different threshold voltage and using a current mirror to serve as current compliance and protect memristors from burnout in writing process. The development of the presented memories is not only based on different models but also measurements done with real devices.

The paper 'Reconfigurable microwave filters using memristors' proposes the use of memristors in RF/microwave reconfigurable filter design. A reconfigurable microwave filter with two pass bands has been proposed for multi-band receiver application using memristor-based switches. The filter has operated in two modes: a single-band bandpass mode and a dual-band bandpass mode. The band-pass filtering has been realized with a planar interdigital structure. Simulation models have been used for (1) exploring memristor-based RF/microwave filters via simulation programs and (2) verifying the expected performance of the proposed reconfigurable filter.

The paper 'Analysis of the Row Grounding Technique in a Memristor Based Crossbar Array' analyzes the row grounding technique and proposes several methods and constraints for the design of memristive crossbar arrays. When the row grounding technique is used for these arrays, the analysis

and simulation show that increasing the number of rows can help reduce read latency and energy, in contrast to the case of capacitive memory arrays.

Although progress has been made in the areas of using memristor for control purposes, there is still a lack of understanding of how the time varying resistance behaviors of memristors affect the dynamic and steady-state performances of a control system, either theoretically or practically, especially for non-linear systems. The paper 'Parameters Self-tuning PID Controller Circuit with Memristors' presents neuron-based self-tuning proportion-integration-differentiation (PID) controllers implemented in a memristor technology. The proposed controller circuits combine a single neuron with a PID algorithm based on voltage-controlled or current-controlled memristors. The mechanisms of the memristor weight update rules and their relationship to the minimization of the output errors of a control system are discussed.

The papers 'Memristor-enhanced humanoid robot control system-Part I: theory behind the novel memcomputing paradigm' and 'Memristor-enhanced humanoid robot control system -Part II: circuit theoretic model and performance analysis' proposes a novel, low-power, time-efficient, and adaptive memristor-centered control strategy for the aforementioned robot action. The idea is based upon the exploitation of the combined ability of memristors to store and process data in the same physical location. The Part I paper sets the theoretic foundations for the mem-computing paradigm to robot motion control, while the Part II manuscript demonstrates its benefits over the original approach in terms of energy, and speed, and the inheritance from the standard strategy of a good level of adaptability to changes in the limb load on the basis of the analysis of circuit-theoretic models adopting an ideal and a real memristor, respectively.

The paper 'Supervised Neural Networks with Memristor Binary Synapses' presents a memristor-based neural network implementing the Stochastic Belief Propagation Inspired algorithm, an efficient supervised learning algorithm (which infers a classification rule from a set of labeled examples) suited for devices with very low-precision synaptic weights.

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